REMARKS

Present Status of the Application

Upon entry of the amendments in this response, claims 5-12 are pending of which claims 5,6,8 and 10-11 have been amended without prejudice or disclaimer in order to more explicitly describe the claimed invention. It is believed that no new matter is added by way of amendments made to the claims. For at least the reasons discussed below, applicants respectfully submit that claims 5-12 patently define over prior art of record and reconsideration of this application is respectfully requested.

Double Patenting

Claim 5 is provisionally rejected on the ground of nonstatutory obvious type double patenting as being unpatentable over claims 1-4, 13,15 of copending application No.09/801,350. They are patentable distinct from each other because applicant's [10/826,725] claim 5 is a combination of the copending application [09/801,350] claims 1, 3 and 4.

In response thereto, applicant respectfully traverses the examiner's allegation double patenting based on the following arguments. After carefully reviewing claim 5 of the present application and the combination of the copending application [09/801,350] claims 1, 3 and 4, we found constitute of anti-latch-up circuit in present application is totally different from that in copending application [09/801,350]. In other words, anti-latch-up circuit in present application is comprised of PMOS transistor, a resistor and a capacitor, rather than of only a resistor and a capacitor in copending application [09/801,350]. Accordingly, as these two applications have different elements in the anti-latch-up circuit, their electrical connections are inherently different. Therefore, these two applications are separate inventions and thus should not be regarded as "double patenting."

Discussion for objection to claims due to informalities

1. *Claim 10 is objected to because in line 6 and 8, "the PMOS transistor" should be "the NMOS transistor"*

In response thereto, applicants have amended claim 10 accordingly.

Discussion for rejection to claims under 35 U.S.C.103 (a)

2. Claim 5 is rejected under 35 U.S.C.103 (a) as being unpatentable over Yu[U.S. Patent 5,869,873],in view of Yu[U.S. Patent 6,031,405]

In response thereto, applicants respectfully traverse the preceding rejection based on the following arguments. To establish a prima facie case of obviousness, the cited references (i.e. YU[PN5,869,873] and YU[PN 6,031,405]) should teach all limitations of the claim 5. The Office Action alleged that the R and C shown in Fig.6 constitute an anti-latch-up circuit as claimed in the amended claim 5. However, from col.5, lines 24-41, in YU[PN5,869,873], there disclose "when ESD stress occurs the pad 1, the capacitor C couples a voltage to the control gate (of an EPROM 4)." Accordingly, in YU[PN5,869,873], the RC circuit is used for coupling ESD stress, not for providing a voltage level for changing the triggering voltage of the SCR circuit, as claimed in the claim 5. Moreover, in YU[PN 6,031,405], an ON/OFF controller 30 is connected to the cathode of the SCR 20; in contrast, from Fig.6A in the present invention, the anti-latch-up circuit 200 is connected to the second N+ doped region 158 that is used a control gate of the SCR circuit for changing a triggering voltage thereof. Therefore, even if YU[PN5,869,873] and YU[PN 6,031,405] could be combined, this combination still fails to teach, suggest or disclose "the second N+ doped region is the third connection terminal of the SCR circuit, which receives the anti-latch-up signal so as to change a triggering voltage of the SCR circuit for preventing its latch-up when the to-be-protected IC is powered by the voltage source," as claimed in the amended claim 5.

Moreover, the connection between SCR and anti-latch-up circuit in the present application is different from that in Yu's [PN5,869,873]. As claimed in the amended claim 5, SCR circuit

has a first and a second terminals connected to the I/O pad and Vss (Ground voltage source) and a third terminal connected to the anti-latch-up circuit, respectively; and the anti-latch-up circuit is connected to Vcc (voltage source, not I/O pad, different from the connection of SCR), Vss and the SCR circuit, respectively. However, in Fig.6, in Yu[PN5,869,873], the RC circuit (used as anti-latch-up circuit) has one terminal connected to the I/O pad (rather than not voltage source in the present application) and the other terminal connected to Vss (ground voltage source) and RC circuit is connected with SCR in parallel; that is, in Yu[PN5,869,873], the terminal of RC circuit (used as anti-latch-up circuit) has the same potential as SCR. However, it is not the same case in the present application.(emphasis added) Namely, the connections of anti-latch-up circuit are different those of the trigger circuit in Yu[PN5,869,873], since the previous one is connected to the voltage source (different from the connection SCR, which is connected to the I/O pad), and the latter one to the I/O pad, which is the same as the connection of SCR (to I/O pad, too).

3. Claim 6 and 8-11are rejected under 35 U.S.C.103 (a) as being unpatentable over Yu [U.S. Patent 5,869,873],in view of Chen[U.S. Publication No. 2001/0007521 A1]

In response thereto, applicants respectfully traverse the preceding rejection based on the following arguments. To establish a prima facie case of obviousness, the cited references (i.e. YU[PN5,869,873] and Chen should teach all limitations of the claims 6 and 8. As discussed above, in YU[PN5,869,873], the RC circuit is used for coupling ESD stress, not for providing a voltage level for changing the triggering voltage of the SCR circuit, as claimed in the claims 6 , 8 and 11. In Chen, although there discloses a NMOS is disposed between two N^+ doped regions, an anti-latch-up circuit is not disclosed at all. Therefore, even if YU[PN5,869,873] and Chen could be combined, this combination still fails to teach, suggest or disclose" the second N+ doped region is the third connection terminal of the SCR circuit, which receives the anti-latch-up signal so as to change a triggering voltage of the SCR circuit for preventing its latch-up when the to-be-protected IC is powered by the voltage source," as claimed in the amended claims 6, 8 and 11. In other words, the amended claims 6, 8 and 11 are not rendered obvious over Yu [U.S. Patent 5,869,873] and further in view of Chen and thus patentable.

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Regarding dependent claims 7-10 and 12, they should be patentable as a matter of law for the reason that they contain all limitations of their corresponding patentable base claims.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 5-12 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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